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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/801,900	03/09/2001	Yutaka Takeishi	A286-1	2596

466 7590 10/24/2003

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EXAMINER	
DI GRAZIO, JEANNE A	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 10/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/801,900	Applicant(s) TAKEISHI ET AL.	
	Examiner Jeanne A. Di Grazio	Art Unit 2871	AU

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

Priority to Japanese Patent Application No. 2000-064532 is claimed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7, 10-19, 20-25, and 28-39 rejected under 35 U.S.C. 103(a) as being unpatentable over Doi (JP-03-116898) in view of Muramatsu et al. (US 5,703,665).

Per claims 1-7, 10-17, 20-25, and 28-36: Doi discloses a volume resistor (16) located on a first printed circuit board (12) where the resistor is capable of easy adjustment (PAJ). An insertion hole (17) opposes the resistor so that the resistor can be adjusted (PAJ). The insertion hole must be appropriately dimensioned so that the resistor can conveniently be adjusted, for example, by the application of a screw driver (PAJ). The variable resistor is also in a floating condition as can be seen in Figure 1 of Doi and the through hole and resistor are aligned in keeping with the ability to adjust resistance. Furthermore, the printed circuit board and substrate have heights relative to each other as can be seen in Figure 1.

Doi does not appear to disclose that the printed circuit board is located on opposite edges of a signal processing circuit substrate; however, Muramatsu teaches that a liquid crystal panel has an interposing unit that is located on the vertices of an isosceles triangle (Col. 1, Lines 52-62).

This arrangement protects the liquid crystal display panel from external stresses (Col. 2, Lines 1-3). Thus, even though the liquid crystal panel may be subjected to external stresses, the panel is ultimately protected from damaging forces because of the aforementioned arrangement.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Doi in view of Muramatsu for a printed circuit board on opposing edges to minimize stress to a signal processing circuit substrate used in an LCD panel.

Per claims 18, 19, 38, and 39: While Doi discloses a volume resistor, the combination of references apply equally to the situation where any electric component, a capacitor or laser trimming resistor, for example, has to be adjusted conveniently and with ease.

Claims 8, 9, 26, and 27 rejected under 35 U.S.C. 103(a) as being unpatentable over Doi (JP-03-116898) in view of Muramatsu et al. (US 5,703,665) and further in view of Asai et al. (US 6,409,159 B1).

Per claims 8, 9, 26, and 27: Doi does not appear to disclose a plate for reinforcing the printed circuit board that absorbs a compressive force exerted on the board when the variable resistor is adjusted; however, Asai teaches a method of supporting a printed circuit board and method of mounting electric components where a member supports the board on a side surface to reduce vibration to the board (Col. 2, Lines 33-35).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Doi in view of Asai to reduce vibration to a printed circuit board.

Claims 40-54 rejected under 35 U.S.C. 103(a) as being unpatentable over Asai et al. (US 6,409,159 B1) in view of Doi (JP-03-116898) and further in view of Muramatsu et al. (US 5,703,665).

Per claims 40-54: Asai discloses a method of mounting printed circuit boards (Col. 2, Lines 24-67). Asai does not appear to have a method of adjusting a variable resistor; however, Doi discloses a volume resistor (16) located on a first printed circuit board (12) where the resistor is capable of easy adjustment (PAJ). An insertion hole (17) opposes the resistor so that the resistor can be adjusted (PAJ). The insertion hole must be appropriately dimensioned so that the resistor can conveniently be adjusted, for example, by the application of a screw driver (PAJ). The variable resistor is also in a floating condition as can be seen in Figure 1 of Doi and the through hole and resistor are aligned in keeping with the ability to adjust resistance. Furthermore, the printed circuit board and substrate have heights relative to each other as can be seen in Figure 1.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Asai in view of Doi for a convenient way of adjusting variable electronic devices as taught in Doi.

Asai does not appear to disclose that the printed circuit board is located on opposite edges of a signal processing circuit substrate; however, Muramatsu teaches that a liquid crystal panel has an interposing unit that is located on the vertices of an isosceles triangle (Col. 1, Lines 52-62).

This arrangement protects the liquid crystal display panel from external stresses (Col. 2, Lines 1-3). Thus, even though the liquid crystal panel may be subjected to external stresses, the panel is ultimately protected from damaging forces because of the aforementioned arrangement.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Asai in view of Muramatsu for a printed circuit board on opposing edges to minimize stress to a signal processing circuit substrate used in an LCD panel.

Remarks

The Terminal Disclaimer filed February 4, 2003 has been accepted.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeanne A. Di Grazio whose telephone number is (703)305-7009. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached on (703) 305-3492. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Jeanne Andrea Di Grazio

JDG

Robert Kim, SPE

T. Chowdhury
Primary Examiner